

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1 1. (Previously Presented) An apparatus, comprising:
2 a first interface;
3 a second interface not directly coupled to said first interface; and
4 a cache accessible from said first interface and said second interface, to
5 contain a cache line, the cache line having two cache coherency states with a
6 first cache coherency state when accessed from said first interface and a
7 second cache coherency state when accessed from said second interface,
8 wherein said first cache coherency state has higher privilege than said second
9 cache coherency state when said second interface is coupled to a processor.

1 2. (Cancelled)

1 3. (Previously Presented) The apparatus of claim 1, wherein said
2 second cache coherency state is to reduce snoop transactions on said second
3 interface.

1 4. (Previously Presented) The apparatus of claim 1, wherein said first
2 cache coherency state is exclusive and said second cache coherency state is
3 shared.

1 5. (Previously Presented) The apparatus of claim 1, wherein said first
2 cache coherency state is modified and said second cache coherency state is
3 shared.

1 6. (Original) The apparatus of claim 3, wherein said second cache
2 coherency state supports speculative invalidation.

1 7. (Original) The apparatus of claim 6, wherein said first cache
2 coherency state is modified and said second cache coherency state is invalid.

1 8. (Original) The apparatus of claim 6, wherein said first cache
2 coherency state is exclusive and said second cache coherency state is invalid.

1 9. (Original) The apparatus of claim 6, wherein said first cache
2 coherency state is shared and said second cache coherency state is invalid.

1 10. (Original) The apparatus of claim 6, wherein said second cache
2 coherency state further supports explicit invalidation.

1 11. (Previously Presented) A method, comprising:
2 associating a first cache coherency state with a first cache line in a first
3 cache, said first cache coherency state being a single cache coherency state,
4 said first cache coupled to a first interface and to a second interface;
5 associating a second cache coherency state with a second cache line in
6 a second cache coupled to said first cache via said second interface;
7 transitioning said first cache coherency state to a joint cache coherency
8 state including said first cache coherency state for said first interface and a third
9 cache coherency state for said second interface; and
10 transitioning said second cache coherency state to said third cache
11 coherency state.

1 12. (Original) The method of claim 11, wherein said first cache coherency
2 state is exclusive, said second cache coherency state is invalid, and said third
3 cache coherency state is shared.

1 13. (Original) The method of claim 11, wherein said first cache coherency
2 state is modified, said second cache coherency state is modified, and said third
3 cache coherency state is invalid.

1 14. (Previously Presented) A method, comprising:
2 associating a first cache coherency state with a first cache line in a first
3 cache, said first cache coherency state being a single cache coherency state,
4 said first cache coupled to a first interface and to a second interface;
5 associating a second cache coherency state with a second cache line in
6 a second cache coupled to said first cache via said second interface;
7 transitioning said second cache coherency state to an invalid state; and
8 transitioning said first cache coherency state to a joint cache coherency
9 state including said first cache coherency state for said first interface and an
10 invalid state for said second interface.

1 15. (Original) The method of claim 14, wherein said first cache coherency
2 state is modified.

1 16. (Original) The method of claim 14, wherein said first cache coherency
2 state is exclusive.

1 17. (Original) The method of claim 14, wherein said first cache coherency
2 state is shared.

1 18. (Previously Presented) A method, comprising:
2 associating a first cache coherency state with a first cache line in a first
3 cache, said first cache coherency state being a single cache coherency state,
4 said first cache coupled to a first interface and to a second interface;
5 associating an invalid state with a second cache line in a second cache
6 coupled to said first cache via said second interface;
7 transitioning said invalid state to a shared state; and

8 transitioning said first cache coherency state to a joint cache coherency
9 state including a shared state for said second interface.

1 19. (Original) The method of claim 18, wherein said first cache coherency
2 state is invalid and said joint cache coherency state is exclusive-shared.

1 20. (Original) The method of claim 18, wherein said first cache coherency
2 state is modified-invalid and said joint cache coherency state is modified-
3 shared.

1 21. (Previously Presented) An apparatus, comprising:
2 means for associating a first cache coherency state with a first cache line
3 in a first cache, said first cache coherency state being a single cache coherency
4 state, said first cache coupled to a first interface and to a second interface;
5 means for associating a second cache coherency state with a second
6 cache line in a second cache coupled to said first cache via said second
7 interface;
8 means for transitioning said first cache coherency state to a joint cache
9 coherency state including said first cache coherency state for said first interface
10 and a third cache coherency state for said second interface; and
11 means for transitioning said second cache coherency state to said third
12 cache coherency state.

1 22. (Original) The apparatus of claim 21, wherein said first cache
2 coherency state is exclusive, said second cache coherency state is invalid, and
3 said third cache coherency state is shared.

1 23. (Original) The apparatus of claim 21, wherein said first cache
2 coherency state is modified, said second cache coherency state is modified,
3 and said third cache coherency state is invalid.

1 24. (Previously Presented) An apparatus, comprising:
2 means for associating a first cache coherency state with a first cache line
3 in a first cache, said first cache coherency state being a single cache coherency
4 state, said first cache coupled to a first interface and to a second interface;
5 means for associating a second cache coherency state with a second
6 cache line in a second cache coupled to said first cache via said second
7 interface;
8 means for transitioning said second cache coherency state to an invalid
9 state; and
10 means for transitioning said first cache coherency state to a joint cache
11 coherency state including said first cache coherency state for said first interface
12 and an invalid state for said second interface.

1 25. (Previously Presented) The apparatus of claim 24, wherein said first
2 cache coherency state is modified.

1 26. (Previously Presented) The apparatus of claim 24, wherein said first
2 cache coherency state is exclusive.

1 27. (Previously Presented) The apparatus of claim 24, wherein said first
2 cache coherency state is shared.

1 28. (Previously Presented) An apparatus, comprising:
2 means for associating a first cache coherency state with a first cache line
3 in a first cache, said first cache coherency state being a single cache coherency
4 state, said first cache coupled to a first interface and to a second interface;
5 means for associating an invalid state with a second cache line in a
6 second cache coupled to said first cache via said second interface;
7 means for transitioning said invalid state to a shared state; and

8 means for transitioning said first cache coherency state to a joint cache
9 coherency state including a shared state for said second interface.

1 29. (Original) The apparatus of claim 28, wherein said first cache
2 coherency state is invalid and said joint cache coherency state is exclusive-
3 shared.

1 30. (Original) The apparatus of claim 28, wherein said first cache
2 coherency state is modified-invalid and said joint cache coherency state is
3 modified-shared.

1 31. (Previously Presented) A system, comprising:
2 a cache accessible from a first interface and a second interface, to
3 contain a cache line, the cache line having two cache coherency states with a
4 first cache coherency state when accessed from said first interface and a
5 second cache coherency state when accessed from said second interface,
6 wherein said first cache coherency state has higher privilege than said second
7 cache coherency state when said second interface is coupled to a processor;
8 a bus bridge to a third interface; and
9 an input-output device coupled to said third interface.

1 32. (Cancelled)

1 33. (Original) The system of claim 31, wherein said second cache
2 coherency state is to reduce snoop transactions on said second
3 interface.